1. A method comprising:

receiving a plurality of data units at a source location in a first clocked domain;

detecting at said first clocked domain, an enable signal to control writing of said plurality of data units from said source location to a target location in a second clocked domain;

synchronizing the enable signal with respect to the second clocked domain; and

in response to said synchronized enable signal, transferring said plurality of data units from the first clocked domain to the target location in said second clocked domain.

2. The method of claim 1, including:

providing a feedback signal to the first clocked domain to indicate at least one of transmission of said plurality of data units and availability of said second clocked domain for the next write cycle.

3. The method of claim 1, including:

providing to said first clocked domain based on the enable signal, a first signal indicating arrival of said plurality of data units of data at the source location;

in response to said first signal, initializing a data transfer of said plurality of data units to the target location in the second clocked domain;

generating a second signal indicating synchronization of said enable signal with respect to said second clocked domain based on the initialization of data transfer;

in response to said second signal, initiating the data transfer from said source location in the first clocked domain to said target location in the second clocked domain;

generating a third signal indicating transmission of said plurality of data units for the first clocked domain based on the initiation of the data transfer; and

in response to said third signal, indicating availability of said second clocked domain to said first clocked domain for a next write cycle.

4. The method of claim 2, further including generating said first signal in response to a transition from a first state to a second state in a state machine.

5. The method of claim 1, including:

providing a first register and an intermediate register being a shadow copy of the first register at the source location in said first clocked domain; and

providing a second register at said target location in said second clocked domain.

6. The method of claim 5, further including loading said plurality of data units into said intermediate register from said first register.

7. The method of claim 4, further including handling switching of a clocking signal based on the state machine while asynchronously transferring said plurality of data units between said first and second clocked domains each domain including at least one independently clocked logic with respect to another clocked logic.

8. The method of claim 7, including providing a synchronizer to enable an asynchronous data transfer between the first and second clocked domains.

9. The method of claim 8, including implementing a protocol causing the transition between said first state and said second state in said state machine to drive said synchronizer.

10. The method of claim 9, including operating said state machine to:

in response to said enable signal, transition from said first state including an initial state to said second state including a plurality of target states according to said protocol;

if at least one condition is met, cause said synchronizer to combine synchronization of said plurality of data units for asynchronous data transfer across said first and second clocked domains; and

if said at least one condition is not met, cause said synchronizer to hold transfer of said plurality of data units.

11. An apparatus, comprising:

a data path coupleable between a first and a second clocked domains; and

a control logic operably coupled to said data path to:

receive a plurality of data units at a source location in a first clocked domain;

detect at said first clocked domain, an enable signal to control writing of said plurality of data units from said source location to a target location in a second clocked domain;

synchronize the enable signal with respect to the second clocked domain; and

in response to said synchronized enable signal, transfer said plurality of data units from the first clocked domain to the target location in said second clocked domain.

12. The apparatus of claim 11, wherein said control logic to provide a feedback signal to the first clocked domain to indicate at least one of transmission of said plurality of data units and availability of said second clocked domain for the next write cycle.

13. The apparatus of claim 12, wherein said control logic to:

provide to said first clocked domain based on the enable signal, a first signal indicating arrival of said plurality of data units of data at the source location;

in response to said first signal, initialize a data transfer of said plurality of data units to the target location in the second clocked domain;

generate a second signal indicating synchronization of said enable signal with respect to said second clocked domain based on the initialization of data transfer;

in response to said second signal, initiate the data transfer from said source location in the first clocked domain to said target location in the second clocked domain;

generate a third signal indicating transmission of said plurality of data units for the first clocked domain based on the initiation of the data transfer; and

in response to said third signal, indicate availability of said second clocked domain to said first clocked domain for the next write cycle.

14. The apparatus of claim 12, further comprising a state machine to generate said first signal in response to a transition from a first state to a second state in said state machine.

15. The apparatus of claim 14, further comprising:

a first register and an intermediate register being a shadow copy of the first register at the source location in said first clocked domain; and

a second register at said target location in said second clocked domain.

16. The apparatus of claim 15, wherein said control logic loads said plurality of data units into said intermediate register from said first register.

17. The apparatus of claim 16, wherein said control logic handles switching of a clocking signal based on the state machine while asynchronously transferring said plurality of data units between said first and second clocked domains each domain including at least one independently clocked logic with respect to another clocked logic.

18. The apparatus of claim 17, further comprising a synchronizer to enable an asynchronous data transfer between the first and second clocked domains.

19. The apparatus of claim 18, further comprising a protocol causing the transition between said first state and said second state in said state machine to drive said synchronizer.

20. The apparatus of claim 19, wherein said protocol operates said state machine to:

in response to said enable signal, transition from said first state including an initial state to said second state including a plurality of target states according to said protocol;

if at least one condition is met, cause said synchronizer to combine synchronization of said plurality of data units for asynchronous data transfer across said first and second clocked domains; and

if said at least one condition is not met, cause said synchronizer to hold transfer of said plurality of data units.

21. An article comprising a medium storing instructions that enable a processor-based system to:

receive a plurality of data units at a source location in a first clocked domain;

detect at said first clocked domain, an enable signal to control writing of said plurality of data units from said source location to a target location in a second clocked domain;

synchronize the enable signal with respect to the second clocked domain; and

in response to said synchronized enable signal, transfer said plurality of data units from the first clocked domain to the target location in said second clocked domain.

22. The article of claim 21, further storing instructions that enable the processor-based system to:

provide a feedback signal to the first clocked domain to indicate at least one of transmission of said plurality of data units and availability of said second clocked domain for the next write cycle.

23. The article of claim 21, further storing instructions that enable the processor-based system to:

provide to said first clocked domain based on the enable signal, a first signal to indicate the arrival of said plurality of data units of data at the source location;

in response to said first signal, initialize a data transfer of said plurality of data units to the target location in the second clocked domain;

generate a second signal to indicate synchronization of said enable signal with respect to said second clocked domain based on the initialization of data transfer;

in response to said second signal, initiate the data transfer from said source location in the first clocked domain to said target location in the second clocked domain;

generate a third signal to indicate transmission of said plurality of data units for the first clocked domain based on the initiation of the data transfer; and

in response to said third signal, indicate availability of said second clocked domain to said first clocked domain for a next write cycle.

24. The article of claim 22, which further storing instructions that enable the processor-based system to generate said first signal in response to a transition from a first state to a second state in a state machine.

25. The article of claim 21, further storing instructions that enable the processor-based system to:

provide a first register and an intermediate register being a shadow copy of the first register at the source location in said first clocked domain; and

provide a second register at said target location in said second clocked domain.

26. The article of claim 25, further storing instructions that enable the processor-based system to load said plurality of data units into said intermediate register from said first register.

27. The article of claim 24, further storing instructions that enable the processor-based system to handle switching of a clocking signal based on the state machine while asynchronously transferring said plurality of data units between said first and second clocked domains each domain including at least one independently clocked logic with respect to another clocked logic.

28. The article of claim 27, further storing instructions that enable the processor-based system to provide a synchronizer to enable an asynchronous data transfer between the first and second clocked domains.

29. The article of claim 28, further storing instructions that enable the processor-based system to implement a protocol causing the transition between said first state and said second state in said state machine to drive said synchronizer.

30. The article of claim 29, further storing instructions that enable the processor-based system to operate said state machine to:

in response to said enable signal, transition from said first state that includes an initial state to said second state that includes a plurality of target states according to said protocol;

if at least one condition is met, cause said synchronizer to combine synchronization of said plurality of data units for asynchronous data transfer across said first and second clocked domains; and

if said at least one condition is not met, cause said synchronizer to hold transfer of said plurality of data units.